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EXAMINER
FENTY, JESSE A

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/27/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N . 09/374,502	Applicant(s) MA ET AL.	
	Examiner Jesse A. Fenty	Art Unit 2815	

-- Th MAILING DATE of this communication appears on the cover sh et with th correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24 and 31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1, 2, 8, 18, 23 and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Wong et al. (U.S. Patent No. 6,083,797).

In re claim 1, Wong (Fig. 2D) discloses a semiconductor device, comprising:

An active area formed in a semiconductor substrate; and

An isolation structure (12) comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area.

The limitation, "wherein at least ... is adapted to ... area" is a recitation of the intended use of the claimed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 2, Wong discloses the device of claim 1, wherein said active area further comprises an NMOS transistor.

In re claim 5, Wong discloses the device of claim 2, wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench having a depth such that an aspect ratio of said trench portion depth to said active area width is greater than about 0.5.

In re claim 8, Wong discloses the device of claim 1, wherein said active area further comprises an PMOS transistor.

In re claims 15 and 20, Wong discloses the device of claim 8, wherein said isolation structure comprises at least a portion of said trench parallel to a channel current direction of the PMOS device components having a depth wherein said active area includes a width and wherein said isolation structure comprises at least a portion of said trench parallel and perpendicular to a channel current direction of the PMOS device having a depth such that an aspect ration of said trench portion depth to said active area width is greater than about 0.5.

In re claim 18, Wong discloses the device of claim 15, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench perpendicular to the channel current direction of the PMOS device components.

In re claim 23, Wong discloses the device of claim 20, wherein said isolation structure comprises a high-modulus, dielectric material disposed within said at least a portion of said trench parallel to the channel current direction of the PMOS device components.

In re claim 31, Wong (Fig. 2D) discloses a semiconductor device, comprising:

An active area formed in a semiconductor substrate; and

A stress modifying isolation structure comprising at least one dielectric material disposed within a trench which extends into said semiconductor substrate, wherein said isolation structure substantially surrounds said active area.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 4, 6, 7, 9-14, 16, 17, 19, 21, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. as applied to claim 2 above, and further in view of Lur (U.S. Patent No. 5,395,790).

In re claims 3, 4, 6 and 7, Wong discloses the devices of claims 2 and 5 respectively, but does not expressly disclose the isolation structure comprising a low-modulus dielectric. Lur discloses an isolation structure using a low-modulus dielectric (polyimide, 29). It would have been obvious to one skilled in the art at the time of the invention to substitute a polyimide dielectric as taught by Lur for the device of Wong for the purpose, for example, solving the problems of crystalline defects or degraded characteristics of devices (Lur; Abstract) which may occur due to lack of stress-reducing support structures.

In re claims 9, 11, 13 and 14, Wong discloses the device of claim 8, but does not expressly disclose the isolation structure comprising a low-modulus dielectric. Lur discloses an

isolation structure using a low-modulus dielectric (polyimide, 29). It would have been obvious to one skilled in the art at the time of the invention to substitute a polyimide dielectric as taught by Lur for the device of Wong for the purpose, for example, solving the problems of crystalline defects or degraded characteristics of devices (Lur; Abstract) which may occur due to lack of stress-reducing support structures. The dielectric material is disposed in the trench both parallel and perpendicular to the channel current direction.

In re claim10, Wong in view of Lur discloses the device of claim 9, wherein said isolation structure comprises a high-modulus, dielectric material (Wong, line 47) disposed within said at least a portion of said trench parallel to a channel current direction of the PMOS device components.

In re claim 12, Wong in view of Lur discloses the device of claim 11, wherein said isolation structure comprises a high-modulus, dielectric material (Wong, line 47) disposed within said at least a portion of said trench parallel to the channel current direction of the PMOS device components.

In re claims 16, 17, 19, 21, 22 and 24, Wong discloses the devices of claims 15 and 20 repsectively, but does not expressly disclose the isolation structure comprising a low-modulus dielectric or tensile-stress inducing dielectric material. Lur discloses an isolation structure using a low-modulus dielectric (polyimide, 29). It would have been obvious to one skilled in the art at the time of the invention to substitute a polyimide dielectric as taught by Lur for the device of Wong for the purpose, for example, solving the problems of crystalline defects or degraded characteristics of devices (Lur; Abstract) which may occur due to lack of stress-reducing support

structures. The dielectric material is disposed in the trench both parallel and perpendicular to the channel current direction.

Response to Arguments

1. Applicant's arguments filed 01/17/02 have been fully considered but they are not persuasive.

Applicant argues that the requirements of 102(e) are not met since Examiner noted that one element of the rejection "can be interpreted" in a certain way. However, as applicant points out, the pertinent section of 102(e) notes "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Though examiner noted in previous Response to Arguments that the STI region of Wong "can be interpreted" to be "high modulus"; this limitation is also met by the *inherency* language of 102(e). The STI region (12) of Wong is *inherently* "adapted to modify stresses incurred in the active area," by the mere placement of the regions in the active area.

Applicant argues that, in regards to claims 1 and 31, that the STI region of the Wong does not surround the active area, not teach such. However, looking at Figure 2D, one skilled in the art will see that the STI region (12) is placed on either side of the active region, as well as in between the N and P channel transistors, thus, surrounding each active region.

The 'intended use" reasoning relied upon by Examiner in previous actions is maintained.

The "stress-modifying" language does not distinguish over the prior art relied upon in the case. Such language must be looked at by Examiner in its broadest possible sense. Any dielectric isolation structure placed in a semiconductor body will be "stress-modifying" If

applicant wishes to differentiate this limitation, more detail must be added, for example, specifying a particular material, a thickness that could not be found by routine experimentation, or a particular density of the material, to name a few.

Applicant argues that Wong does not expressly teach an aspect ration of 0.5. However, as interpreted by Figure 2 of Wong and the dimension information (column 4, lines 31-65), one skilled in the art, through routine experimentation would have been able to compute an aspect ratio in the range claimed in the present invention.

Lastly, in response to the argument that the secondary reference, Lur, does not disclose the present invention. Applicant argues that while the "polyimide" of Lur is not expressly disclosed as low-modulus, Examiner notes that there is no teaching that the polyimide is not low-modulus. The body of the specification teaches that polymer substances are low-modulus. Polyimide is a polymer and in the absence of data showing that such a material is not low-modulus, one skilled in the art would readily make the correlation between the two materials. Secondly, though Lur discloses that the isolation material to be "stress-free", this does not ineffectuate the teachings of Lur. Third, Lur does not disclose the isolation structure surrounding the active area; but Lur is not relied upon for that purpose. The device of Wong clearly demonstrates that claim limitation.

Conclusion

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 703-308-8137. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 703-308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-746-3892 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Jesse A. Fenty
Examiner
Art Unit 2815

JAF
August 25, 2002

EDDIE LEE
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